Defining and Overcoming the Contact Resistance Challenge in Scaled Carbon Nanotube Transistors

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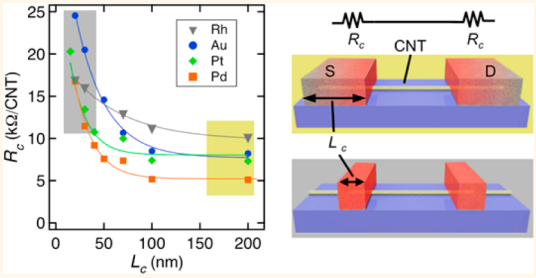
ABSTRACT Carbon nanotubes (CNTs) continue to show strong promise as the channel material for an aggressively scaled, high-performance transistor technology. However, there has been concern regarding the contact resistance (R_c) in CNT field-effect transistors (CNTFETs) limiting the ultimate performance, especially at scaled contact lengths. In this work, the contact resistance in CNTFETs is defined in the context of a high-performance scaled transistor, including how the demonstrated R_c relates to technology targets. The impact of different source/drain contact metals (Pd, Pt, Au, Rh, Ni, and Ti) on the scaling of R_c *versus* contact length is presented. It is discovered that the most optimal contact metal at long contact lengths (Pd) is not necessarily the best for scaled devices, where a newly explored scaled metal contact, Rh, yields the best scaling trend. When extrapolated for a sub-10 nm transistor technology, these results show that the R_c in scaled CNTFETs is within a factor of 2 of the technology target with much potential for improvement through enhanced understanding and engineering of transport at the metal–CNT interface.



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Scaling down the size of silicon metal-oxide–semiconductor field-effect transistors (MOSFETs) has been carried out for decades in order to increase the density of devices on a chip and provide better computational performance. In the past 10 years, the inability to correspondingly reduce the operating voltage (V_{DD}) for MOSFETs as they shrink has led to major bottlenecks in device performance for recent transistor technologies.[1−4] To deliver the needed performance metrics at the device densities of the sub-10 nm technology nodes (*ca.* 2020 and beyond), a transistor must be able to operate at $V_{DD} \leq 0.5$ V. The inability to reduce V_{DD} in Si-based devices has led to an intensifying search for a new transistor channel material or device;[5−7] one of the foremost options is single-walled carbon nanotubes (CNTs).

CNTs offer the ideal 1D channel for transistors, as they are intrinsically 1D (quantum confinement is part of their natural physical structure), extremely thin (~1 nm diameter), and semiconducting (band-gap range of approximately 500–800 meV, inversely dependent on diameter) and exhibit ballistic transport at room temperature.[8,9] Through the years, there have been many demonstrations of CNT field-effect transistors (CNTFETs) with superb performance, including complementary devices,[10,11] gate-all-around devices,[12−14] and devices with channel lengths scaled to ~9 nm.[15,16] In addition to the 9 nm channel length CNTFET displaying promising performance at $|V_{DD}| = 0.5$ V,[15] there have also been circuit demonstrations of complementary CNT-driven logic gates operating at $V_{DD} < 0.5$ V.[10,17] There have also been advancements in the purification of semiconducting CNTs and their precise positioning in parallel arrays,[18−23] showing promise for achieving the target purity and placement density by the 2020 time frame.[24] While this device- and material-related progress is impressive and motivating, there remains confusion regarding what will determine the performance in a technologically compatible CNTFET.

Carrier transport through a CNT channel is ballistic for a channel length (L_{ch}) below approximately 40 nm, as demonstrated by

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several groups over the years.[8,9,25] This means that for the total measured resistance in a device, R_{tot}, the contribution from the channel is effectively zero. Hence, contact resistance, R_c, determines the performance of scaled CNTFETs. A few years ago, it was shown that R_c increases with decreasing contact length,[9] L_c (the length over which the contact metal covers a CNT). This contact resistance-related scaling behavior is not unique for CNTs but is also a major factor for Si and III−V MOSFETs.[26] To follow the current technology node trend, scaling down L_c is as crucial as scaling L_{ch}, regardless of the transistor material. By the 2020 time frame, a channel length of ~10 nm is expected with a contact length of the same order, ranging from 7 to 14 nm depending on whether or not a contact is shared between gates. Efforts have been made to improve understanding of transport at the metal−CNT contact to improve the L_c scaling behavior,[27−30] but a complete model is still lacking and further progress requires more experimental evidence of transport behavior. What is completely missing from the community is a clear definition of what constitutes the contact resistance in a CNTFET and how it relates to the target R_c for sub-10 nm technologies.

In this work, we define R_c in CNTFETs as the resistance attributed to one contact for one CNT (kΩ/CNT) and show how it relates to the technology-relevant, device-level $R_{c\text{-}DEV}$ (Ω·μm). Because a CNTFET will require several parallel CNT channels (just as FinFETs require several Fins), the impact of the density of parallel CNTs (CNTs/μm) on the target R_c is also explored. To improve understanding of transport at metal−CNT contacts, the scaling behavior of six different metal contacts is studied: Ti, Ni, Rh, Au, Pt, and Pd. Interestingly, the metal that provides the lowest R_c at long contact lengths (>100 nm) is not necessarily the best choice for scaled contacts (<20 nm) based on the revealed scaling trends. This unique scaling behavior presented by the different metal−CNT contacts provides crucial insight for the ultimate CNTFET at sub-10 nm technologies. Extrapolating the best CNTFET R_c *vs* L_c trend to the target L_c range reveals that CNTFETs are within a factor of 2 of the $R_{c\text{-}DEV}$ technology target.

RESULTS AND DISCUSSION

While the majority of reported CNTFETs have only a single CNT channel, a technologically viable device will require several parallel CNT channels in order to deliver the needed drive current.[31] This is not unique to CNTs, as the same is true for any nanowire or FinFET device. The basic layout for a CNTFET is shown in Figure 1a, with six parallel channels, metal source/drain contacts, and a local bottom gate, as has been demonstrated previously.[9,15,31] A simple model was built to fit the experimental data of a single-channel CNTFET with a 9 nm channel length (see Supporting Information for details of the model), the shortest channel length

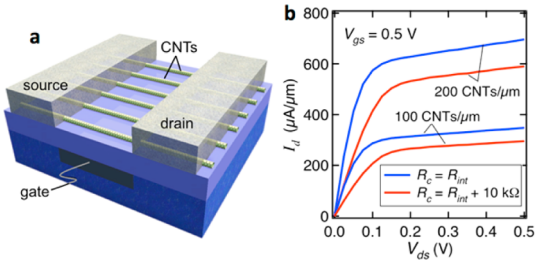

Figure 1. Impact of contact resistance and CNT density in a CNTFET with parallel CNT channels. (a) Schematic of a CNTFET with the channel comprising parallel CNTs at a certain pitch, metal source/drain contacts, and an embedded bottom gate. (b) Simulated output characteristics for the device in (a) at a certain density of CNTs per micrometer width of the device (CNTs/μm). Curves are shown for two different R_c scenarios: blue [quantum limit where the only R_c is from the intrinsic resistance (R_{int} is the quantum resistance (R_q = 3.25 kΩ/contact) divided by the number of transport modes) and R_{ext} = 0] and red [external contact resistance at the metal−CNT junction of R_{ext} = 10 kΩ/contact].

reported to date.[15] Using this model, the drain current (I_d) *versus* drain−source voltage (V_{ds}) curves were generated for different contact resistance scenarios.

In a transistor technology, the on-state value that matters most when considering a device for its scalability and performance is the current per device width (μA/μm), which makes different device technologies comparable independent of design details. With multiple parallel CNT channels, the pitch of the CNTs will determine the density in CNTs/μm. Note that if CNTs are too closely packed together, then there will be adverse charge screening effects that degrade the gate control of electron flow.[32−34] The minimum distance would be an approximately 5 nm pitch—recall that CNTs have a diameter of ~1 nm—yielding 200 CNTs/μm. The on-state output curves for 100 and 200 CNTs/μm are given in Figure 1b for two different R_c scenarios. As will be discussed further below, R_c is made up of two components in CNTFETs, an intrinsic (R_{int}) and an extrinsic (R_{ext}) resistance. In Figure 1b, the impact of R_{ext} is illustrated by showing the performance at R_{ext} = 0 and R_{ext} = 10 kΩ per CNT. Note that R_c is for a single contact in the two-contact device, where the total contact resistance would be $2R_c$.

With the basic device structure defined, along with a visualization of the impact of R_c on performance, a more detailed picture of the contact resistance is now considered. The contact resistance in traditional MOSFETs is most commonly defined as the measured resistance multiplied by the device width. We will denote this resistance $R_{c\text{-}DEV}$, with units of Ω·μm. Each projected transistor technology has a certain target $R_{c\text{-}DEV}$ for achieving the needed performance metrics. The meaning of $R_{c\text{-}DEV}$ for CNTFETs is detailed in Figure 2. From the schematic in Figure 2b, each CNT has a corresponding R_c (kΩ/CNT) per contact. As illustrated, the device $R_{c\text{-}DEV}$ is then the CNT R_c divided by the density of parallel CNT channels (CNTs/μm), which is

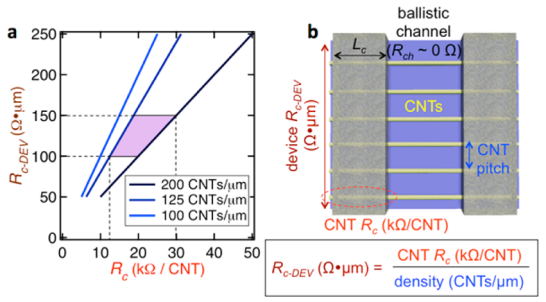

Figure 2. Relationship between target device $R_{c\text{-}DEV}$ and CNT R_c. (a) Device contact resistance in traditional units of Ω·μm *versus* contact resistance per CNT plotted at three different CNT pitches: 10, 8, and 5 nm. The projected device R_c range for a sub-10 nm high-performance transistor technology is indicated, defining the range of CNT R_c that must be targeted with dependence on pitch. (b) Top-view schematic of a CNTFET illustrating the relevant contributions to contact resistance and how the individual CNT R_c relates to the overall device $R_{c\text{-}DEV}$. Also defined is the contact length, L_c.

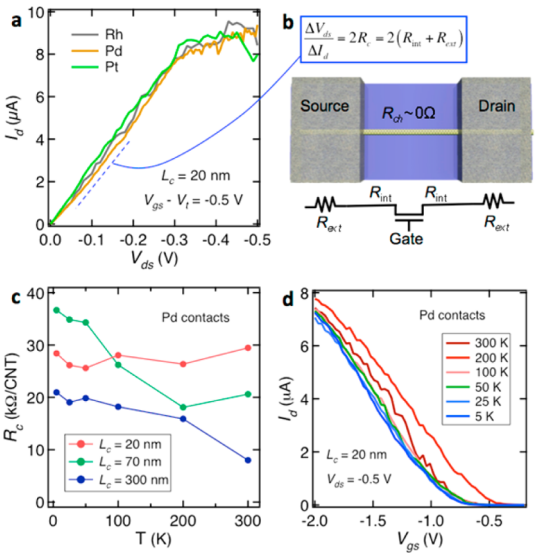

Figure 3. Extraction of CNT R_c from output characteristics and temperature dependence. (a) Output curves (I_d *vs* V_{ds}) for scaled devices with Rh, Pd, and Pt contacts, each with a single CNT channel. The gate overdrive is $V_{gs} - V_t = -0.5$ V, and all devices are at the same channel length L_{ch} = 40 nm. Extraction of the CNT R_c is illustrated, coming from the linear, low-field slope of the curves before the onset of current saturation. (b) Breakdown of R_c into an intrinsic (quantum resistance) and extrinsic component at each contact. (c) Temperature dependence of R_c for three different contact lengths using Pd contacts. (d) Transfer curves across the tested temperature range for the L_c = 20 nm device showing consistent on-state performance.

determined by the CNT pitch, yielding Ω·μm. The target range for $R_{c\text{-}DEV}$ in a sub-10 nm technology is 100−150 Ω·μm,[35] as indicated in Figure 2a. For a CNT pitch between 5 and 8 nm (125−200 CNTs/μm), the target CNT R_c range would be 12−30 kΩ/CNT. This target range for $R_{c\text{-}DEV}$ is from the projections in the International Technology Roadmap for Semiconductors (ITRS) and is independent of the transistor channel material, which could be Si or III−V or CNTs, because it represents the spatial resistance of the device.

It is critical to note that the CNT R_c (in Figure 2) contains both an intrinsic and extrinsic component. This is illustrated in Figure 3a,b, where the extraction of R_c from experimental output curves of devices with three different contact metals is shown. With a channel length of 40 nm, these devices have ballistic channels (R_{ch} ~0), so the measured low-field slope is attributed entirely to the contacts: $2R_c$ for both contacts. The R_{int} component is the fundamental quantum resistance ($R_{int} = R_q = 3.25$ kΩ divided by the number of transport modes), which is constant and results from interfacing with a quantum confined system.[36] The remainder of the measured resistance is R_{ext} and arises from the injection and transport of carriers at the metal−CNT contact. As demonstrated in Figure 1b, R_{ext} can considerably impact the device performance and is the resistance that shows dependence on contact length, as will be discussed next.

To achieve increased transistor integration densities, scaling down the size of the contacts is as crucial as scaling the channel length, but has received much less attention. For a sub-10 nm technology, L_c (as defined in Figure 1b) will need to be on the order of 10 nm with a channel length of ~10 nm (see discussion above). Hence, it is crucial to consider the scaling behavior of metal−CNT contacts for determining which metal is best and how close present devices are to the technology $R_{c\text{-}DEV}$ target. To date, only one study experimentally explores the impact of L_c scaling on R_c for CNTFETs, and it focuses on Pd contacts.[9] The result was an approximately $1/L_c$ scaling trend for R_c below $L_c \approx 50$ nm.

Five new contact metals (Ti, Ni, Rh, Pt, and Au) are studied in this work and compared to the Pd scaling behavior. Each of these metals has been considered in previous CNTFET studies,[8,37−40] but this is the first exploration of the contact scaling behavior for each. All CNTFETs had a single CNT channel and a back gate geometry with L_{ch} = 40 nm. For each contact metal, a series of devices with varying L_c was assembled along the same CNT so as to maintain the same diameter and, hence, a consistent band gap among the devices. Example output curves at L_c = 20 nm from devices with Rh, Pd, and Pt contacts are given in Figure 3a at the same gate overdrive, which is how much gate-source voltage (V_{gs}) is applied beyond the device threshold voltage (V_t). For all devices, R_c was extracted from the low-field slope of the output curve at $V_{gs} - V_t = -0.5$ V. Temperature dependence of R_c was also studied for Pd contacts, as shown in Figure 3c,d. In Figure 3c, consider the nonmonotonic change in R_c from 300 to 20 nm (with deviation in the 70 nm case) and the roughly constant value of R_c at 20 nm. This signifies that, though it may be present, the Schottky barrier does not exclusively define the performance of the devices, playing a diminished role. This highlights the new

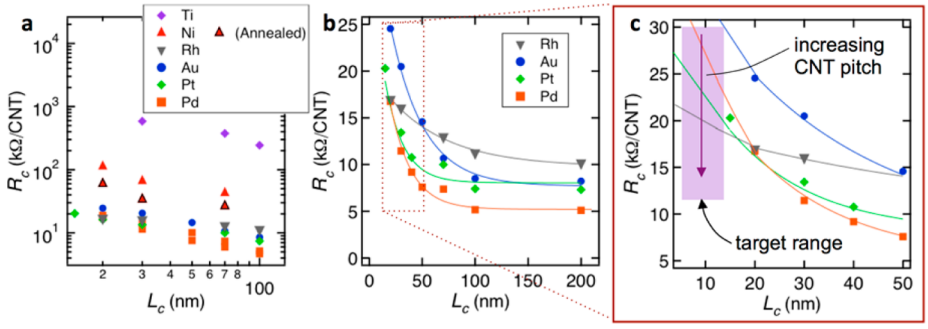

Figure 4. Scaling trend of contact resistance *versus* contact length for six different metals. (a) All metals from this study are shown using a log−log scale, with Ni showing improvement following a 12 h anneal in vacuum at 350 °C. For each contact metal, the set of data points comes from devices assembled along a single CNT. (b) Linear scale plot showing the four metals with the lowest R_c, including Rh, Au, Pt, and Pd. (c) Closer view of the scaling trends at small contact lengths, highlighting the target range based on the analysis in Figure 2, spanning 6 nm < L_c < 15 nm and 12 kΩ < R_c < 30 kΩ. Note that this range depends on CNT pitch, which is assumed to be between 5 and 8 nm. All R_c values are extracted at a gate overdrive of $V_{gs} - V_t = -0.5$ V.

device transport regime entered by L_c scaling that will be discussed further below.

The R_c *versus* L_c scaling trends for the six studied contact metals are shown in Figure 4. Note that R_c for the Ti and Ni devices was so high that the Figure 4a plot is given on a log−log scale in order to show all of the data. The yield of Ti devices was extremely low, likely due to oxidation of the contacts affecting the metal−CNT interface. Because Ni has been shown to provide excellent contact to graphene after annealing,[41] the Ni devices were tested before and after a 350 °C anneal in vacuum. While R_c in the Ni devices did improve with the anneal, it was still considerably higher than for the Rh, Au, Pt, and Pd devices. Regarding the R_c data in Figure 4, for each contact metal studied the given data are from a set of CNTFETs assembled along a single CNT channel with varying L_c and consistent $L_{ch} = 40$ nm. The CNTs used were tens of micrometers in total length, grown by chemical vapor deposition (CVD) on quartz substrates and transferred to the device substrate. For information on the use of solution-processed CNTs for studying L_c scaling and details of variation among the studied devices, see the Supporting Information. The range for R_c values broadens as L_c is scaled, which suggests that residual resist and other debris become more impactful to the metal−CNT interface when that interface length is small, an intuitive observation. Choosing the set of CNTFETs with the lowest R_c values for each contact metal is most useful, as it represents the best, cleanest interface between the metal and CNT.

A linear scale illustrates the R_c *vs* L_c scaling behavior more clearly, as shown in Figure 4b,c. The smallest L_c achieved in this work is ∼15 nm for a Pt contact device and ∼20 nm for all other metals. As discussed from Figure 2a, the target range for R_c (based on the target $R_{c\text{-}DEV}$) is highlighted in Figure 4c and shows that the trends for Pd, Pt, and Rh all fall within the upper portion of the range, which would be for the highest density of CNTs (∼5 nm pitch). The shaded box in Figure 4c indicates the contact length target range of interest and the required R_c range with respect to the CNT pitch: the upper portion of the R_c target range is for small pitch (5 nm), while the lower bound is for larger pitch (8 nm). A less aggressive, and more accessible, CNT pitch would be 8−10 nm (100−125 CNTs/μm) and would require a ∼2× reduction in R_c at the scaled lengths.

One of the most important observations from the Figure 4b,c trends is that the contact metal that yields the lowest R_c at long L_c does not necessarily scale the best. For years it has been known that Pd contacts provide p-type CNTFETs with the best and most uniform performance.[8,37,38] The next most common contact with nearly comparable performance has been Au. Though only demonstrated a few times, Pt has generally proven to be sporadic in whether it offers decent performance or a low device yield attributed to its poor wetting of the CNT surface. Even though Rh contacts exhibited the highest R_c at long lengths (∼2× the R_c of Pd contacts), the scaling behavior for Rh is much more favorable, which infers that the Rh−CNT contact has a smaller transfer length (L_T). L_T is the length of the contact over which the majority of the applied potential is dropped, or the length over which nearly all of the carriers are injected from the metal to the CNT.[42] A smaller L_T will allow greater immunity to contact scaling. The best example of a difference in L_T is seen with the Au and Pt data in Figure 4b; R_c for both contact metals is nearly the same at long L_c, but the difference in L_T is clearly seen as the contacts are scaled. Also note that the R_c for the Pd, Pt, and Rh devices at $L_c = 20$ nm in Figure 3a is nearly identical; yet below 20 nm these contact metals yield distinctly different scaling behavior.

All of the devices studied in this work were operated as p-type CNTFETs, where a negative V_{gs} and V_{ds} bias constitute the on-state. For a p-type device, holes are injected into the valence band from the source; hence the negative voltages serve to lower the injection

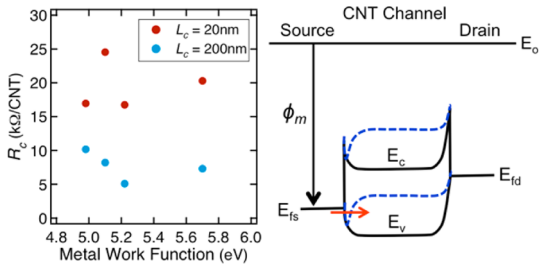

Figure 5. Impact of metal work function on contact resistance. Plot of the contact resistance *versus* metal work function ϕ_m of the source/drain contacts at two different contact lengths. A qualitative illustration of the band diagram for a CNTFET is shown for both the off-state (black bands) and on-state (dashed blue bands) under an applied V_{ds} at the drain.

barriers for hole transport. While a discussion of how the contact metal work function impacts the operation of these devices is below, it is important to note that there is no inclusion in this study of low work function metals. Other reports have shown that employing low work function metals—including Er,[43] Y,[44] and Sc[45]—creates a favorable situation for electron injection into the conduction band, yielding n-type CNTFETs with superb performance at long L_c. Whether such low work function metals exhibit the same scaling behavior that is observed for the p-type devices studied in this paper remains unknown. In this study, we explored the scaling behavior of Er contacts to CNTs but were unsuccessful at yielding any functioning devices at contact lengths below ~70 nm, which was attributed to the rapid oxidation of the metal diminishing the actual contact length due to lateral oxidation. When the contact lengths are small, oxidation of the contact from both ends can have a dramatic impact on the effective contact length. In order for a reliable study of the n-type contact scaling behavior in CNTFETs to be accomplished, first the challenge of rapid oxidation of low work function metal contacts must be resolved.

Transport at metal−CNT contacts has been almost exclusively interpreted using a Schottky barrier (SB) injection model. While such a model has provided an explanation for CNTFET operation at long L_c,[37,46−48] the data from this study indicate that this does not hold at scaled contact lengths. Consider the data plotted in Figure 5, where the metal work function (ϕ_m) for each contact is assumed to be the clean ϕ_m; there can be fluctuation in ϕ_m depending on the environment, interface, *etc*. As indicated in the simple qualitative energy band diagram in Figure 5, a high ϕ_m will bring the Fermi level in the source (E_{Fs}) closer to the valence band edge (E_v), thus lowering the SB height and allowing for more efficient carrier injection. At L_c = 200 nm, this expected trend does generally hold, with the moderate exception being Pt (ϕ_m ~5.7 eV). However, at L_c = 20 nm the trend is changed dramatically and shows no clear dependence of R_c on ϕ_m, indicating that the SB model for a CNTFET no longer captures the complexities of carrier transport at scaled lengths.

With the metal work function not providing sufficient explanation for the scaling behavior of metal−CNT contacts, there is a need for theorists to revisit the transport physics in scaled CNTFETs. Additionally, further experimental work will help to improve the understanding of how the physical metal−CNT interface affects scalability. Previous studies on longer contacts have pointed to the wetting or coupling of a metal to a CNT surface, typically using molecular dynamics simulations.[30,49] To truly understand the interface will require a detailed study of how the different metals coat the inert CNT surface. Other interesting follow-up studies to these new results would be to consider the impact of interfacial layers between the metal and CNT and how they impact L_c scaling. While some work on interfacial layers has been done,[39] there has not been any consideration of how they impact R_c *vs* L_c. It is also important to note that the technological requirements at the sub-10 nm nodes will include the need for making scaled metal contacts that are manufacturable, with device characteristics having a very low variability in key metrics such as threshold voltage. Finally, there are reports that the best metal−CNT contact would come from an end-contact rather than side-contact.[50] All of the contacts in this study are side-contacts in that the metal is interacting with the inert sp^2 carbon surface. An end-contact would be a metal interacting with the dangling carbon bonds at the opened end of a CNT, forming chemical bonds. There has yet to be experimental evidence of a truly edge-contacted CNTFET—there is tremendous difficulty in keeping the dangling bonds from having unwanted molecular attachments prior to contact metallization—but perhaps such a geometry could help in reaching the ultimate R_c target at scaled L_c.

CONCLUSIONS

In conclusion, the contact resistance in CNTFETs has been defined in the context of a high-performance transistor technology at the sub-10 nm technology nodes. The impact of R_c on CNTFET performance was demonstrated. It was shown that the target R_c for CNTFETs is dependent on the pitch of the parallel CNT channels in a device and that current experimental data are projected to be within ~2× of the technology target at a pitch of 5−8 nm (125−200 CNTs/μm). The scaling behavior of six different metal−CNT contact interfaces was presented, revealing that the contact metal with the lowest R_c at long L_c does not provide the best scaling behavior. Rh exhibited the most promising R_c *vs* L_c scaling trend with the smallest transfer length. Furthermore, it was shown that the Schottky barrier model by which CNTFET transport has been interpreted through the years does not

sufficiently describe scaled L_c devices; contact metal work function does not noticeably contribute to R_c at small lengths. In addition to clarifying the contact resistance picture for CNTFETs, these results suggests that experimental devices have R_c within a factor of 2 of the technology targets with much work to be done to understand and improve transport at scaled metal–CNT interfaces.

METHODS

Local Bottom Gate Fabrication on 200 mm Wafers. In a 200 mm silicon production fab, beginning with intrinsic Si wafers, 1 μm thick SiO_2 was thermally grown at 1050 °C in a wet oxidation furnace. The wafer was then spin-coated with photoresist and patterned using an ASML Deep UV stepper. High-power reactive ion etching with a mixture of CHF_3 and Ar for 150 s was used to remove ~350 nm SiO_2 followed by photoresist stripping in oxygen plasma. Tungsten (W) was then sputter deposited to a thickness of ~500 nm, filling the trenches and coating the wafer. Next, the wafer was polished to planarize the W in a Westech CMP system. HfO_2 (50 Å) was then deposited at 200 °C in a Cambridge Nanotech Fiji atomic layer deposition system to cover the whole wafer, and an HBr-based RIE process was used to etch open the contact pad to the gate. The Pd and Ti contacted CNTFETs in this study were assembled on these local bottom gates, whereas the Ni, Pt, Rh, and Au contacted CNTFETs were on p^+-doped Si substrates with 10 nm SiO_2 and used the doped substrate as the back gate. Despite the difference in gate dielectric, devices from both geometries exhibited no short channel effects at the ~40 nm channel length.

Carbon Nanotube Growth and Transfer. The carbon nanotubes were grown on ST-cut quartz substrates annealed overnight in air at 900 °C and then coated with a resist containing a suspension of iron catalyst particles.[51] The resist was patterned into catalyst strips using optical lithography. CNT growth was then carried out in a 2 in. diameter tube furnace at 900 °C for 10 min by running forming gas (95% Ar/5% H_2) through an ethanol bubbler chilled to 0 °C, yielding an average of 1 CNT/μm, intentionally low so as to isolate long, individual CNTs. The aligned nanotube arrays were then transferred to either the local bottom gate substrates or 10 nm SiO_2 on doped Si substrates (see above). Transfer of the CNTs was achieved by coating them with 100 nm Au using an electron beam evaporator, then peeling them from the quartz substrate using thermal tape (RevAlpha 3198M) as described elsewhere.[9,52] After applying the CNT/Au/tape structure to the Si substrate, a brief baking on a 130 °C hot plate delaminated the thermal tape. A 5 min clean in an O_2 plasma was used to remove the residue from the tape from the Au surface, and then the Au was etched away in standard Au etchant (Transene TFA) for 3 min 30 s.

Device Fabrication. After the CNTs were transferred to the Si substrates, electron beam lithography (EBL) was used to pattern the source/drain contacts in poly(methyl methacrylate) (PMMA) resist, after which electron beam evaporation was used to deposit the contact metals of the following thicknesses: Ti (5 nm Ti/20 nm Au), Ni (20 nm Ni), Pd (0.2 nm Ti/20 nm Pd), Au (0.2 nm Ti/20 nm Au), Pt (0.2 nm Ti/20 nm Pt), and Rh (0.2 nm Ti/20 nm Rh). Use of the 2 Å Ti underlayer for the Pd, Au, Pt, and Rh contacts was to promote adhesion of the high work function metals; the deposited Ti is too thin to form a monolayer and rather yields inhomogeneous Ti nanoparticles that help to adhere the subsequent metal films to the substrate. The resist was then lifted-off in hot acetone. The source/drain contacts were patterned in sets that contained six devices that were designed to be along a single CNT channel. All six devices in a set had the same L_{ch} = 40 nm with varying L_c from 15 to 200 nm. All data reported here are from devices in the same set (on the same CNT channel) for each contact metal. Next, EBL was used to pattern resist to protect the area of the nanotube channel (designed to be 300 nm wide so as to capture nominally one nanotube for each device); the exposed CNTs were then etched away using an O_2 plasma, and the resist was removed in acetone. Finally, EBL and electron beam evaporation were used to pattern and deposit contact leads and pads of 1 nm Ti/20 nm Pd/30 nm Au.

Electrical Characterization. Electrical characterization was carried out in air, with no additional passivation or annealing treatments. First, a Cascade semiautomated probe station was used to rapidly test for semiconducting CNTs in the devices. Once the semiconducting devices were identified, more detailed electrical measurements were performed using a Lakeshore probe station along with an Agilent B-1500 semiconductor parameter analyzer.

Conflict of Interest: The authors declare no competing financial interest.

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Supporting Information Available: Detailed information on the model used to generate data for Figure 1b, use of solution-processed CNTs for L_c scaling, discussion of variation in L_c-scaled devices, and additional temperature dependence data. This material is available free of charge *via* the Internet at http://pubs.acs.org.

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